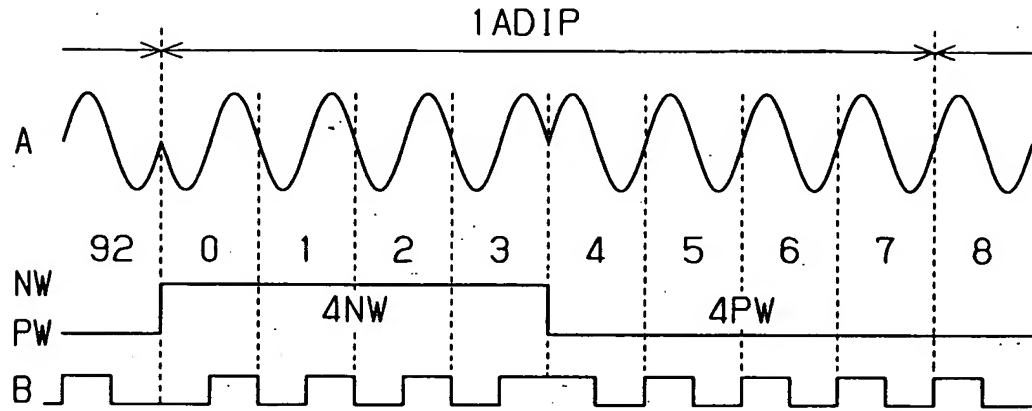
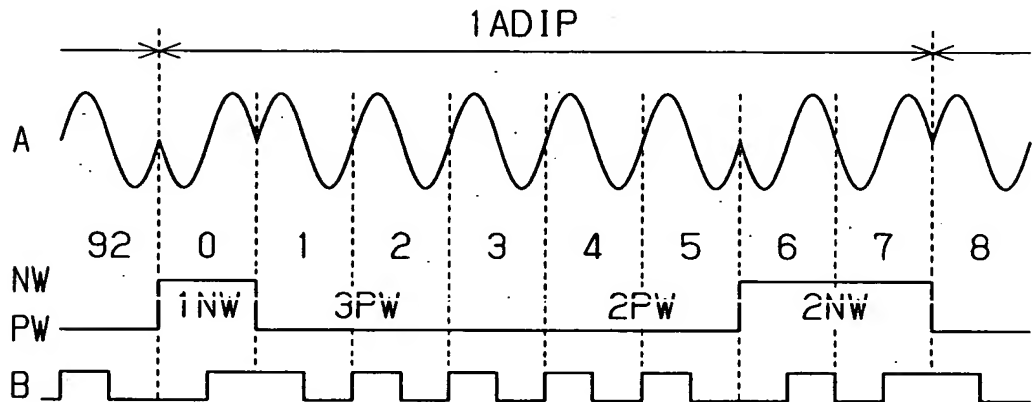
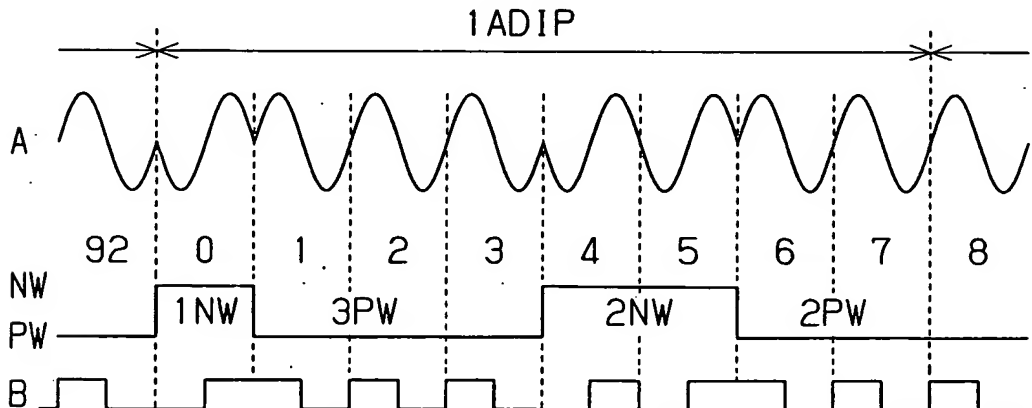


**Fig.1 (a) (Prior Art)****Fig.1 (b) (Prior Art)****Fig.1 (c) (Prior Art)**

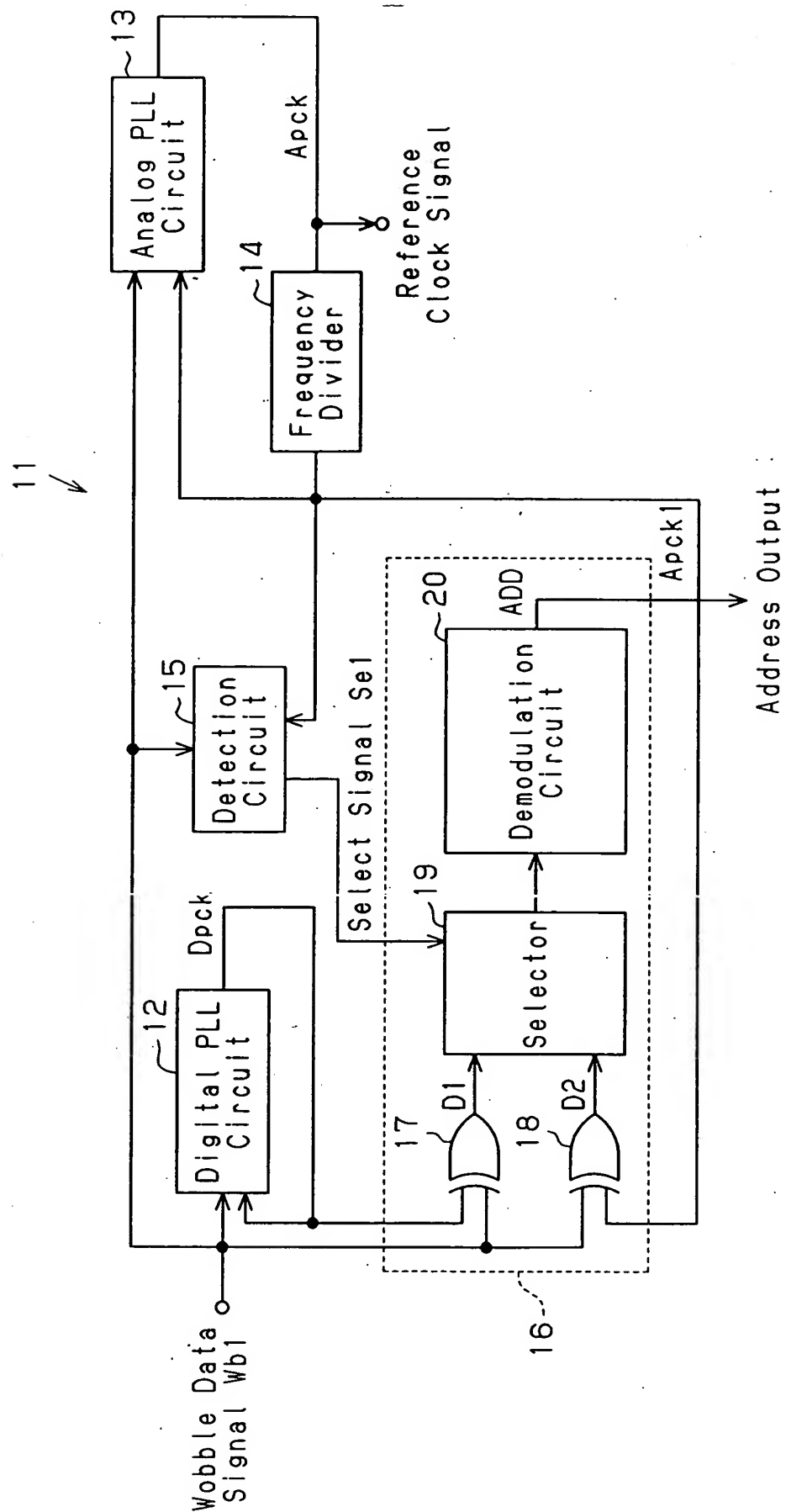
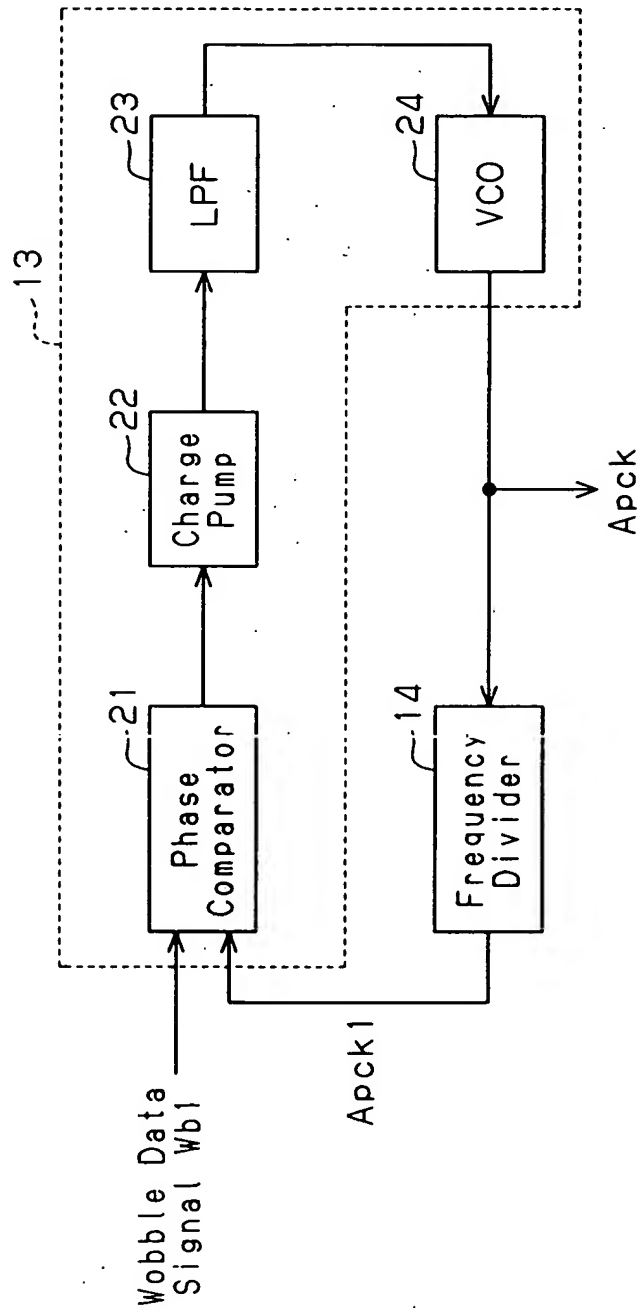
**Fig. 2**

Fig.3



Applicant(s): Hideki Hirayama

DECODER HAVING ANALOG PLL CIRCUIT AND DIGITAL  
PLL CIRCUIT**Fig. 4**